AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A process for a semiconductor integrated circuit device where a plurality of memory cells which have field effect transistors formed in a semiconductor substrate and capacitor elements connected to the source and drain regions of said field effect transistors are provided, comprising the steps of:

(a) forming trenches of which the radius of curvature of the bottom corners is larger than 10nm in a first semiconductor region of said semiconductor substrate;

(b) forming a first gate insulating film through a deposition method inside of said trenches; ~~and~~

(c) forming gate electrodes within said trenches and placing said gate electrodes on said first gate insulating film; and

(d) forming a second semiconductor region and a third semiconductor region in said first semiconductor region such that said second and said third semiconductor regions have a depth shallower than that of said first semiconductor region and that of said trenches,

wherein said second and said third semiconductor regions serve as source and drain regions of said field effect transistor such that a channel forming region thereof is effected at the bottom surface of said trench and two side surfaces of said trench between said second semiconductor region and said third semiconductor region.

2. (Original) A process for a semiconductor integrated circuit device according to Claim 1 characterized by having the step of forming a second gate insulating film by oxidizing the inner walls of said trenches.

3. (Original) A process for a semiconductor integrated circuit device according to Claim 1, wherein the step of forming said trenches contains the step of carrying out an etching process by switching to etching conditions of rounding the corner parts within the trenches during the etching process proceeding in the direction of the trench depth after carrying out an etching process under etching conditions of relatively strong anisotropy.

4. (Currently Amended) A process for a semiconductor integrated circuit device, ~~at the time of forming~~ including field effect transistors ~~in a semiconductor substrate~~, comprising the steps of:

(a) forming trenches in ~~said~~ a first semiconductor region of a semiconductor substrate;

(b) forming a gate insulating film inside of said trenches;

(c) forming gate electrodes which are completely, or partially, buried within said trenches under the condition where said gate insulating film is interposed between said gate electrodes and said semiconductor substrate within said trenches; ~~and~~

(d) forming semiconductor regions for the sources and drains in said semiconductor substrate[[,]] ; and

(e) forming a second semiconductor region and a third semiconductor region in said first semiconductor region such that said second and said third

semiconductor regions have a depth shallower than that of said first semiconductor region and that of said trenches,

wherein said second and said third semiconductor regions serve as said source and said drain regions of a field effect transistor such that a channel forming region thereof is effected at the bottom surface of said trench and two side surfaces of said trench between said second semiconductor region and said third semiconductor region, and

wherein said Step (a) contains the step of rounding the bottom corners within said trenches so that the sub-threshold coefficient of said field effect transistors does not exceed a predetermined value, and said Step (b) contains the step of forming said gate insulating film through a deposition method.

5. (Original) A process for a semiconductor integrated circuit device according to Claim 4, wherein said Step (a) contains the step of carrying out an etching process by switching to etching conditions of rounding the corner parts within the trenches during the etching process proceeding in the direction of the trench depth after carrying out an etching process under etching conditions of relatively strong anisotropy.

6. (Original) A process for a semiconductor integrated circuit device according to Claim 4, wherein said Step (b) contains the step of forming part of said gate insulating film by oxidizing the inner walls of said trenches.

7. (Original) A process for a semiconductor integrated circuit device according to Claim 4, wherein the radius of curvature of the bottom corners within

said trenches is 10nm or more.

8. (Original) A process for a semiconductor integrated circuit device which has element isolation parts and wires formed so as to cross over said element isolation parts within a semiconductor substrate are provided, comprising the steps of:

(a) forming a first trench in said semiconductor substrate;

(b) forming element isolation parts by forming an insulating film in said first trench;

(c) forming a mask which has apertures crossing over said element isolation parts;

(d) forming a second trench in the element isolation parts which have been exposed through said apertures;

(e) forming a third trench in the semiconductor substrate which has been exposed through said apertures and the second trench; and

(f) forming said wires in said second and third trenches.

9. (Original) A process for a semiconductor integrated circuit device according to Claim 8, wherein the inclination angle of the side walls of said first and third trenches, with respect to the main surface of said semiconductor substrate, is smaller than 90 degrees.

10. (Original) A process for a semiconductor integrated circuit device which has element isolation parts formed within a semiconductor substrate, a first wire formed so as to cross over said element isolation parts and field effect

transistors having part of said first wire as gate electrodes and having source and drain regions on both sides of said gate electrodes are provided, comprising the steps of:

(a) forming a first trench by etching said semiconductor substrate;

(b) forming element isolation parts by forming an insulator film inside of said first trench;

(c) forming a mask which has first apertures formed so as to cross over said element isolation parts;

(d) forming a second trench by etching the element isolation parts which have been exposed through said first apertures;

(e) forming a third trench by etching the semiconductor substrate which has been exposed through said first apertures and said second trench; and

(f) forming a gate insulating film on the inside walls of said third trench and forming the first wire inside of said second and third trenches.

11. (Original) A process for a semiconductor integrated circuit device according to Claim 10, wherein the inclination angle of the side walls of said first and third trenches, with respect to the main surface of said semiconductor substrate, is smaller than 90 degrees.

12. (Original) A process for a semiconductor integrated circuit device according to Claim 10, wherein forward tapers are formed on the side surfaces of said first and third trenches.

13. (Original) A process for a semiconductor integrated circuit device according to Claim 10, wherein said first trench is 100nm, or more, deeper than said second trench.

14. (Original) A process for a semiconductor integrated circuit device according to Claim 10, wherein said step of forming the third trench further contains the step of oxidizing the inner walls of the trench formed through etching of said semiconductor substrate and the step of removing the oxide film formed according to said oxidation.

15. (Original) A process for a semiconductor integrated circuit device according to Claim 10, wherein said third trench is deeper than said second trench.

16. (Original) A process for a semiconductor integrated circuit device according to Claim 10, wherein said first trench is deeper than said third trench.

17. (Original) A process for a semiconductor integrated circuit device is provided, comprising the steps of:

(a) forming a first trench in a semiconductor substrate;

(b) forming isolation parts by forming an insulating film for isolation in said first trench;

(c) forming a mask having aperture parts which expose both of said isolation parts and said semiconductor substrate on said semiconductor substrate;

(d) forming a second trench in the isolation parts which have been exposed from said aperture parts and, after that, forming a third trench in the semiconductor

substrate which has been exposed from said aperture parts and said second trench;

(e) forming an insulating film on the surface of the semiconductor substrate within said second and third trenches; and

(f) forming wires within said second and third trenches.

18. (Original) A process for a semiconductor integrated circuit device according to Claim 17, wherein at the time of forming said second trench, at the stage after said Step (f), said insulating film for isolation remains at the bottom of said second trench so that no parasitic elements are formed below the wires formed inside of said second trench.

19. (Original) A process for a semiconductor integrated circuit device according to Claim 17, wherein at the stage after said Step (f), the thickness of said insulating film for isolation which remains between the wires inside of said second trench and the semiconductor substrate is 100nm or more.

20. (Original) A process for a semiconductor integrated circuit device according to Claim 17, wherein at the time of forming said third trench, the depth of said third trench is deeper than said second trench.

21. (Original) A process for a semiconductor integrated circuit device according to Claim 17, wherein the dimensions of the aperture sides of said first and third trenches are greater than the dimensions of the bottom sides.

22. (Original) A process for a semiconductor integrated circuit device according to Claim 21, wherein forward tapers are formed on the side surfaces of said first and third trenches.

23. (Original) A process for a semiconductor integrated circuit device according to Claim 17 characterized by having the oxidation step for oxidizing the inside of said second and third trenches after said Step (d) and before said Step (e) and the step of removing the oxide film which has been formed through said oxidation step.

24. (Original) A process for a semiconductor integrated circuit device according to Claim 23, wherein said Step (e) contains the step of forming said insulating film through a deposition method.

25. (Original) A process for a semiconductor integrated circuit device according to Claim 23, wherein the process for forming an insulating film in said Step (e) contains the step of forming a first gate insulating film by oxidizing the surface of said semiconductor substrate and the step of forming a second gate insulating film, through a deposition method, so as to cover the surface of said first gate insulating film.

26. (Original) A process for a semiconductor integrated circuit device according to Claim 17, wherein said step of forming wires comprises the steps of: filling in said second and third trenches with a first film for forming said wires; removing said first film so that a part thereof remains inside of said second and third

trenches; forming a second film which fills in the recesses of the surface of the first film which has remained inside of said second and third trenches; and removing said first film, after the formation of said second film, so that a part thereof remains inside of said second and third trenches.

27. (Original) A process for a semiconductor integrated circuit device according to Claim 26 characterized by having the step of forming a first insulating film on the wires inside of said second and third trenches by removing the first insulating film so that a part thereof remains inside of said second and third trenches after depositing the first insulating film on said semiconductor substrate subsequent to the formation of said wires.

28. (Original) A process for a semiconductor integrated circuit device according to Claim 27 characterized by having the step of depositing a second insulating film on said semiconductor substrate after forming said first insulating film inside of the second and third trenches, and forming holes which expose part of said semiconductor substrate in said second insulating film, wherein:

in said step of forming holes, said holes are formed by carrying out an etching process under conditions where the etching rate of said second insulating film is faster than that of said first insulating film.

29. (Original) A process for a semiconductor integrated circuit device according to Claim 28, wherein after filling in said holes with a conductive film, semiconductor regions are formed in a semiconductor substrate through impurity diffusion into the semiconductor substrate from the conductive film.

30. (Original) A process for a semiconductor integrated circuit device according to Claim 17, wherein said wires have a polycrystal silicon film, a silicide film or a metal film, or a laminated film of these.

31. (Original) A process for a semiconductor integrated circuit device according to Claim 17, wherein the insulating film of said Step (e) forms a gate insulating film for field effect transistors while the wires of said Step (f) form gate electrodes for said field effect transistors.

32. (Original) A process for a semiconductor integrated circuit device according to Claim 17 characterized by having the step of forming pairs of semiconductor regions for sources and drains of said field effect transistors in an active region surrounded by the isolation parts of said semiconductor substrate after said Step (f) and the step of forming capacitor elements for information storage which are connected to either one of the semiconductor regions of said pairs.

Claim 33 (Canceled).

34. (Currently Amended) A process for a semiconductor integrated circuit device which has a plurality of memory cells having field effect transistors with buried gate electrodes formed in a semiconductor substrate and capacitor elements electrically connected to at least one of the source or drain regions of said field effect transistors are provided, comprising the steps of:

(a) forming first semiconductor regions in said semiconductor substrate;

(b) forming a first trench in said semiconductor substrate;

(c) forming a gate insulating film, gate electrodes and a first insulating film inside said first trench;

(d) forming a second insulating film on the semiconductor substrate and, further, ~~on~~ over said first insulating film;

(e) forming apertures, in said second insulating film, which overlap said first semiconductor regions in a plane manner through a method where the etching rate of said second insulating film is faster than the etching rate of the first insulating film;

(f) forming a conductive film inside of said apertures; and

(g) forming second semiconductor regions in said semiconductor substrate through an impurity diffusion from said conductive film ~~and of forming said source and drain regions of~~ such that said first and second semiconductor regions serve as said source and drain regions.

35. (Original) A process for a semiconductor integrated circuit device according to Claim 34, wherein said first insulating film is formed of a silicon nitride film and said second insulating film is formed of a silicon oxide film.

Claims 36-50 (Canceled).

51. (New) A method of manufacturing a semiconductor integrated circuit, comprising steps of:

(a) forming an element isolation region in a first semiconductor region of a semiconductor substrate such that said element isolation region defines a first region of said first semiconductor region so as to surround said first region;

(b) forming a trench in said first semiconductor region and in said element

isolation region such that said trench crosses said first region;

(c) forming a gate insulating film of a field effect transistor on said first semiconductor region inside of said trench;

(d) after said step (c), burying a gate electrode of said field effect transistor into said trench;

(e) after said step (d), introducing an impurity in said first region in self-alignment with said element isolation region and said gate electrode so as to form a second semiconductor region and a third semiconductor region in said first semiconductor region such that said second and said third semiconductor regions have a depth shallower than that of said first semiconductor region and that of said trench,

wherein said second and said third semiconductor regions serve as said source and said drain region of said field effect transistor such that a channel forming region thereof is to be formed at the bottom surface of said trench and two side surfaces of said such trench between said second semiconductor region and said third semiconductor region.

52. (New) A method of manufacturing a semiconductor integrated circuit according to claim 51, wherein said step (b) includes substeps of:

(b1) etching said element isolation region to form a first trench in said element isolation region; and

(b2) after said substep (b1), etching said first semiconductor region to form a second trench in said first region.

53. (New) A method of manufacturing a semiconductor integrated circuit according to claim 52, wherein a depth of said second semiconductor region is uniform within said source and drain region such that an entire circumference of the bottom of said second semiconductor region contacts the element isolation region or said trench.

54. (New) A method of manufacturing a semiconductor integrated circuit according to claim 51, wherein a depth of said second semiconductor region is uniform within said source and drain region such that an entire circumference of the bottom of said second semiconductor region contacts the element isolation region or said trench.

55. (New) A method of manufacturing a semiconductor integrated circuit according to claim 4, wherein a depth of said second semiconductor region is uniform within said source and drain region such that an entire circumference of the bottom of said second semiconductor region contacts the element isolation region or said trench.

56. (New) A method of manufacturing a semiconductor integrated circuit according to claim 1, wherein a depth of said second semiconductor region is uniform within said source and drain region such that an entire circumference of the bottom of said second semiconductor region contacts the element isolation region or said trench.